REMARKS

Applicants appreciate the detailed examination evidenced by the Office Action mailed April 4, 2005 (hereinafter "Office Action"). Applicants have amended independent Claim 1 to recite "a phase interpolator circuit that receives a reference clock signal and generates a finely variably delayed clock signal therefrom responsive to a first control signal," and "a variable delay circuit that receives the finely variably delayed clock signal and generates a coarsely variably delayed output clock signal therefrom responsive to a second control signal," a combination of fine and coarse delay components that are neither disclosed nor suggested by any of the cited references. Applicants have also amended independent Claim 14 to recite a phase interpolator circuit comprising "a delay circuit configured to receive a reference clock signal" and "a phase interpolator that interpolates between an input and an output of a delay of the delay circuit responsive to the control input to produce a phase interpolated clock signal," recitations that are also neither disclosed nor suggested by any of the cited references.

Applicants have also canceled Claims 2, 8, 9, 21, 22 and 27-29. The cancellations of Claims 9 and 22 obviate the objections to the drawings. Applicants have further added new Claim 29 to depend from amended independent Claim 1. Reasons supporting patentability of the claims as amended are provided below.

Independent Claim 1 is patentable

As noted above, Claim 1 has been amended to recite a particular arrangement of a fine variable delay phase interpolator and a coarse variable delay circuit, thus including subject related to Claim 8. The Office Action implies that U.S. Patent Application Publication 2004/0158757 (hereinafter "Lin I"), U.S. Patent No. 6,281,726 to Miller, Jr. (hereinafter "Miller"), and U.S. Patent No. 6,604,775 to Saitoh et al. (hereinafter "Saitoh") do not disclose or suggest a phase interpolator circuit that "receives the reference clock signal and produces a phase interpolated clock signal therefrom" and a variable delay circuit that "receives the phase interpolated clock signal and generates the output clock signal therefrom," as recited in Claim 8. Applicants note that Lin I and Saitoh each describe phase and/or delay locked loops in which a coarse variable delay unit feeds a fine variable delay unit. Applicants

further note that Miller does not even show a cascade of coarse and fine delays; rather, the cited FIG. 3 of Miller shows a delay locked loop that produces separate in-phase and quadrature clock signals CLKOUT(90°) and CLKOUT(180°), but has no apparent coarse and fine adjustment capability.

In rejecting Claims 8 and 22, the Office Action solely relies on U.S. Patent No. 6,836,166 to Lin et al (hereinafter "Lin II") as allegedly teaching "the phase interpolator precedes the variable delay circuit." Office Action, p. 4. The cited FIG. 2 of Lin II does show parallel delay paths 202, 204 that include fine delay line and control elements 210, 218 that precede coarse delay line and control elements 216, 220. However, careful examination of FIG. 2 reveals that a base coarse variable delay line 208 precedes these paths 202, 204. The base coarse variable delay line 208 receives a buffered clock signal CLKBUF, which is also applied as the reference input to a phase detector 228. Responsive to buffered clock signal CLKBUF and a feedback clock signal CLKFB, the phase detector 228 generates a coarse delay adjustment signal CDADJ that is applied to the base coarse variable delay line 208 and a fine delay adjustment signal FDADJ that is applied to a fine adjustment control logic block 214 that controls the paths 202, 204.

Thus, Lin II shows a coarse variable delay unit that precedes a fine delay unit made up from the paths 202, 204, each of which provide two levels of fine delay resolution. If, as alleged in the Office Action, the phase detector 228 and the fine adjustment control logic 214 are construed as corresponding to the recited "phase control circuit" of Claim 1, the fine delay line and control elements 210, 218 do not receive the buffered clock signal CLKBUF applied to the phase detector 228; rather, the buffered clock signal CLKBUF is applied ***to the base coarse variable delay line 208***. Accordingly, among other things, Lin II does not disclose or suggest "a phase interpolator circuit that receives a reference clock signal and generates a finely variably delayed clock signal therefrom responsive to a first control signal," as recited in Claim 1. Such teachings are also absent from the other cited references, as discussed above. For at least these reasons, Applicants submit that amended independent Claim 1 is patentable over all of the cited references.

Independent Claim 14 is patentable

As noted above, independent Claim 14 has been amended to recite:

A DLL circuit, comprising:
a phase interpolator circuit comprising:
a delay circuit configured to receive a reference clock signal; and
a phase interpolator that interpolates between an input and an output of one delay of the delay circuit responsive to the control input to produce a phase interpolated clock signal;
a tapped delay chain circuit configured to receive the phase interpolated clock signal and to generate a delayed output signal therefrom responsive to the control input; and
a phase control circuit that generates the control input responsive to a comparison of the output clock signal to the reference clock signal.

None of the cited references discloses or suggests a phase interpolator that applies its output to a tapped delay chain circuit. As discussed above, Lin I shows a tapped delay line followed by a interleaved fine delay line, Saitoh shows a coarse tapped delay line followed by a fine tapped delay line, Lin II shows a base coarse tapped delay line followed by two finer tapped delay lines, and Miller shows two separate tapped delay lines that are not in the same loop. For at least these reasons, Applicants submit that amended independent Claim 14 is patentable.

Moreover, Applicants submit that none of the references disclose or suggest a phase interpolator circuit that includes "a phase interpolator that interpolates between an input and an output of one delay" (recitations that are supported, for example, by FIGs. 2 and 3 and the accompanying description on p. 5 of the specification). In particular, page 3 of the Office Action cites the interleaved fine delay line 99 of FIG. 9 of Lin I as corresponding to the recited phase interpolator. However, none of the structures shown in FIGs. 3-7 as being potential constituents of such an interleaved fine delay line 99 include "a phase interpolator that interpolates between an input and an output of a delay." Such features are also absent from the fine delay line and control 210 shown in FIG. 2 of Lin II, which is also alleged to correspond to the recited phase interpolator. See Office Action, p. 4. The interpolation circuitry 50 of FIG. 3 of Miller, cited on page 5 of the Office Action as corresponding to the recited phase interpolator, also lacks such features, as can be seen in FIG. 4. Turning to

Saitoh, the cited fine stepsize delay 12, also alleged to correspond to the recited phase interpolator on page 6 of the Office Action, also does not interpolate "between and input and an output of a delay." For at least these additional reasons, Applicants submit that independent Claim 14 is patentable.

The dependent claims are patentable

Applicants submit that the dependent claims are patentable at least by virtue of the various ones of independent Claims 1 and 14 from which they depend. Applicants submit that several of the dependent claims are separately patentable. For example, Claim 5 recites "wherein the phase control circuit is operative to cause the phase interpolator circuit to shift from one extreme of a delay range thereof towards another extreme of the delay range concurrent with a step change in delay through the variable delay circuit." The Office Action cites FIG. 3 of Miller as providing such teachings. In particular, the Office Action asserts that the counters 44 and 54 cause the interpolation circuitry 50 (the alleged "phase interpolator circuit") to shift from one extreme of delay range to another extreme of delay range concurrent with a step change in delay of the z delay elements 42 and associated mux 46 (the alleged "variable delay circuit"). However, the counters 44, 54 appear to merely track one another such that, when one of the clocks output by the delay elements 42 is selected by the mux 46 (i.e., a step change in delay), a corresponding one of the clocks output by the interpolation circuitry 50 is selected by the mux 52. Thus, there appears to be no shift between *extremes* of a delay range of the interpolation circuitry 50 concurrent with a step change delay provided by the delay elements 42 and mux 46. For at least this reason, Applicants submit that Claim 5 is separately patentable over Miller. Applicants submit that Claim 18 is separately patentable over Miller for at least similar reasons.

The Office Action also cites FIG. 10 of Saitoh as allegedly teaching the above-mentioned recitations of Claim 5. However, the Office Action indicates that "step changes in the fine delay circuit is concurrent with step change the variable delay circuit." Office Action, p. 7. This is not what Claim 5 recites; Claim 5 recites a change between *extremes* of delay range of the phase interpolator circuit concurrent with a step change in delay through the variable delay circuit. For at least this reason, Applicants submit that Claim 5 is separately

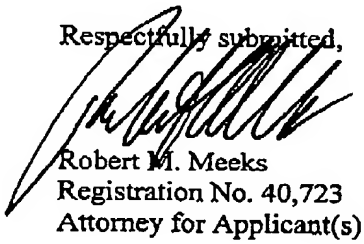
patentable over Saitoh. Applicants submit that Claim 18 is separately patentable over Saitoh for at least similar reasons.

Applicants further note that new dependent Claim 29 is separately patentable for at least similar reasons to those discussed above with reference to Claim 14.

Conclusion

Applicants submit that the rejections of the claims and the objections to the specification have been overcome for at least the reasons provided above, and that the claims are now in condition for allowance. Applicants request allowance of the claims and passing of the application to issue in due course. Applicants encourage the Examiner to contact the undersigned by telephone to resolve any remaining issues.

Respectfully submitted,



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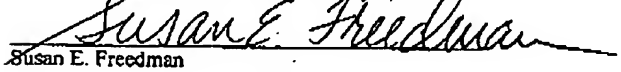

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Date of Signature: July 1, 2005